line 3, delete "from" and insert -- by accessing --;

line 4, delete "a unit transfer time in a time shared fashion" and insert -- said memory cycle --.

Claim 48, lines 1-2, delete "the graphic data" and insert -- said successive groups of m bits of data --;

line 2, after "controller" insert -- through said first bus -- also after "is" and insert -- combined to from n bits of data and --;

line 4, delete "unit transfer time" and insert -- said memory cycle --.

IN THE ABSTRACT:

Line 6, delete "serial" and insert -- sequential --;

line 7, delete "each" and insert -- the --.

and insert.

REMARKS

Minor amendments were made to the Abstract to more clearly describe the invention.

Attached herewith is a Supplemental Reissue Declaration executed by the inventors and the assignee of the present application.

Claims 1-12, 14, 16, 18-34 and 44-48 stand as being based on a defective Reissue Declaration under 35 USC §251. Particularly, the Examiner alleges that the Reissue

Declaration filed on May 11, 1993 is defective because it lacks precise statements distinctly specifying the excess or the insufficiency in the claims, because it fails to particularly specify the areas relied upon and because it fails to particularly specify how the errors relied upon arose or occurred. The attached Supplemental Reissue Declaration addresses these issues raised by the Examiner. Therefore, this rejection is overcome and should be withdrawn. Reconsideration and withdrawal of this rejection is respectfully requested.

Claims 20, 22, 28-34 and 42 stand rejected under 35 USC §251 being that the Examiner alleges that the claims are not directed to the invention disclosed in the original application. Particularly, the Examiner alleges that claims 21, 22, 28-34 and 42 are directed to a method wherein the specification indicates that the invention is an apparatus. Although the originally filed application discloses the invention as an apparatus the method claims are not directed to a method entirely different from the functions performed by each of the elements of the apparatus. In fact the method claims merely recite the functions performed by each of the means recited in the claims of the originally filed application. Therefore, the method claims are in fact directed to the same invention as that of the original application. For example, in claim 21 the reading out, converting and applying steps correspond to the functions performed by the interface means or the memory control means recited in the apparatus claims. Thus, it is quite clear

that the method claims includes steps which correspond to the functions performed by the means recited in the apparatus claims. Therefore, the method claims are directed to the same invention as that disclosed in the originally filed application.

The Examiner further rejects claims 14, 18, 19, 24, 25, 28-34, 36, 37, 39, 42, 43, 47 and 48 under 35 USC §251 as not being directed to the same invention disclosed in the original application. Particularly, the Examiner alleges that these claims are directed to accessing memory within predetermined time periods while the invention disclosed in the originally filed application is for an apparatus having the disclosed architecture in order to reduce the size and cost of the apparatus. The Examiner is in error in this regard being that the specification clearly describes that the reduction in size and cost of the apparatus is "an object of the invention" and that in order to obtain the object the present invention provides a data converting means between processor which processes parallel data and a memory so as to enable the data bus width of the memory to be smaller than that of the processor. These features of the invention as disclosed in the originally filed application are recited in claims 14, 18, 19, 24, 25, 28-34, 36, 37, 39, 42, 43, 47 and 48. These claims do not merely recite that they are directed to accessing memory within a predetermined time period as alleged by the Examiner but in fact also recite that the bus connected between the processor and the memory control means/interface means has a

bit width of n bits, that the bus connected between the memory and the memory control means/interface means has a bit width of m bits and that n is greater than m. The above-described apparatus which was disclosed in the originally filed application so as to achieve the object of the present invention is disclosed in column 1, lines 53-62 of the present application which corresponds to the originally filed application. Thus, claims 14, 18, 19, 24, 25-28, 34, 36, 37, 39, 42, 43, 47 and 48 are directed to the same invention disclosed in the original application.

Therefore, in light of the above, Applicants traverse the Examiner's rejection of claims 14, 18, 19, 20, 22, 24, 25, 28-34, 36, 37, 39, 42, 43, 47 and 48 under 35 USC §251 and respectfully request the Examiner to reconsider and withdraw this rejection.

Claims 1, 2, 8-12, 14, 16, 18-24 and 44-48 stand rejected under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Various amendments were made throughout claims 1, 2, 8-12, 14, 16, 18-34 and 44-48 to bring them into conformity with the requirements of 35 USC §112, second paragraph. Therefore, Applicants submit that this rejection is overcome and should be withdrawn.

Specifically, amendments were made throughout the claims to overcome the objections noted by the Examiner in paragraphs 7a-7i of the Office Action. However, with respect to 7b it is submitted that the language is quite

clear as to the precise scope and meaning thereof. Particularly, the language recites that m bit terminals or n bit terminals are provided. Thus, if n is 4 then the language in the claims would read 4 bit terminals whereas if n is 16 then the claim would read 16 bit terminals. Bit terminals are terminals which extend from the apparatus wherein one bit of data is applied to each bit terminal.

The Examiner's cooperation is respectfully requested to contact Applicants' Attorney by telephone should any further indefinite matter be discovered so that appropriate amendments may be made.

Claims 4-7 stand rejected under 35 USC §102(3) as being anticipated by Lumelsky. This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now recited in claims 4-7 are not taught or suggested by Lumelsky whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to claims 4-7 in order to more clearly describe features of the present invention. Particularly, claims 4-7 were amended so as to more clearly conform to the features of the present invention illustrated in Fig. 1. For example, claim 4 recites a graphic processing apparatus including memory means 30, data processing means 10, memory control means 20 and output means 40. As now recited in claim 40 the memory means

stores pixel information, the data processing means specifies addresses of memory locations in the memory means for retrieval of pixel information therefrom and processing the retrieved pixel information and the memory control means is coupled to the memory means and the data processing means for retrieving pixel information from the memory means in response to a request to retrieve pixel information from the data processing means at the specified addresses, applying the retrieved pixel information to the data processing means for processing thereof, receiving processed pixel information from the data processing means and storing processed pixel information in the memory means.

The other element of the present invention as recited in claim 4 is that the output means is connected to the memory control means and outputs processed pixel information to generate graphics. These features of the present invention are not taught or suggested by Lumelsky.

Lumelsky merely provides a pixel data path for high performance raster displays. Particularly, Lumelsky provides an apparatus which allows selective operations in an attached all points addressable (APA) frame buffer. Lumelsky teaches that operations may be performed on multiple pixels, multiple pixel slices or a single plane bit position in multiple pixels.

The apparatus to which Lumelsky is directed is illustrated in Fig. 1 wherein a video display adapter is shown having a digital signal processor which manages the overall adapter resources, an instruction and data storage

block 12 having instructions and codes to enable operation of the digital signal processor 10, a command FIFO 14 which serves as an input buffer for passing sequential commands to the digital signal processor 10, a pixel processor 18 which contains logic that performs a number of pixel operations and a frame buffer 20. The Examiner alleges that the memory control means is illustrated in Figs. 8-11 and 15-17. Lumelsky clearly describes that the apparatus illustrated in Fig. 8 is a pixel data path coprocessor architecture structured primarily for pixel operations, Fig. 9 illustrates a similar apparatus, Fig. 10 illustrates a plane channel and Fig. 11 illustrates a data informatter. Fig. 15 illustrates a data out formatter, Fig. 16 illustrates a control circuits which facilities color antialiasing and Fig. 17 illustrates a data path architecture.

In light of the above-noted teachings of Lumelsky, Applicants fail to find any teaching or suggestion of a memory control means as recited in the claims of the present application. Further, Applicants submit that the elements of the present invention pointed by the Examiner as being taught by Lumelsky are not connected in the same manner as that of the present invention recited in claims 4-7.

Claims 4-7 of the present application have been amended in the manner described above, so as to more clearly recite that the memory control means retrieves pixel information from the memory means in response to the data processing means, applies the retrieved pixel information to the data processing means, receives processed pixel information from

the data processing means and stores processed pixel information in the memory means. Such features are clearly not taught or suggested by Lumelsky.

Even further, Applicants fail to find any teaching or suggest in Lumelsky wherein the output means is connected directly to the memory control means and outputs processed pixel information provided therefrom as in the present invention.

Therefore, Applicants submit that the features of the present invention as recited in claims 4-5 are not taught or suggested by Lumelsky whether taken individually or in combination with any o the other references of record.

Claims 1-3, 8-12, 14, 16, 18-34 and 44-48 stand rejected under 35 USC §103 as being unpatentable over Graciotti. This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now recited in claims 1-3, 8-12, 14, 16, 18-34 and 44-48 are not taught or suggested by Graciotti whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to the claims in order to more clearly recite that the present invention is particularly directed to the retrieving and storage of data in a memory wherein the memory is connected to a data bus of m bits and the data processor which performs processing operations on data retrieved from or to be stored in the memory is

connected to a data bus having n bits where n is > m. In order to accomplish the accessing of memory in such an environment, the present invention provides a memory control means/interface means which converts the n bits of data into successive groups of m bits of data and applies or retrieves the successive groups of m bits of data to and from the memory by performing plural write or read operations in the memory within a memory cycle. Such features are not taught or suggested by Graciotti.

Graciotti is merely directed to the conversion of an 16 bit data bus to an 8 bit data bus so as to allow connection of a processor having a 16 bit data bus to a peripheral having an 8 bit data bus. Applicants fail to find any teaching or suggestion in Graciotti as to how the data on the bus connected to a memory is to be manipulated so as to retrieve or store bits of data to and from the data processor as in the present invention. In the present invention the memory controller means/interface means performs successive retrievals of groups of m bits of data from the memory within a memory cycle when retrieving data from the memory and sequentially stores successive groups of m bits of data to the memory when data is to be stored in the memory. Such operations are clearly not taught or suggested by Graciotti.

The above-described features of the present invention are further emphasized by, for example, the recitation in claims 1-3 and 8 wherein row and column addresses are manipulated in such a manner such that a plurality of column

addresses are applied to the memory in a single row so as to retrieve or store the successive groups of m bits of data. Such operations are clearly not taught or suggested by Graciotti.

Further, Applicants fail to find any teaching or suggestion in Graciotti that such sequential retrieval or storage of groups of m bits of data are accomplished within a memory cycle as recited in the claims of the present application. This feature of the present invention is illustrated, for example, in Fig. 6 of the present application wherein the FD signal illustrates 4 successive retrievals/storage of data which occur within the second portion of an MCYC signal. Such a feature of the present invention is not taught or suggested by Graciotti.

The Examiner alleges that Graciotti teaches that the system disclosed therein changes a 16 bit memory access into two bit memory accesses within a predetermined time. The Examiner has not pointed to where such teaching can be found in Graciotti. In fact, Applicants, upon complete review of Graciotti, fail to find any such teaching therein.

In light of the above, Applicants submit that the features of the present invention as now recited in the claims are not taught or suggested by Graciotti whether taken individually or in combination with any of the other references of record.

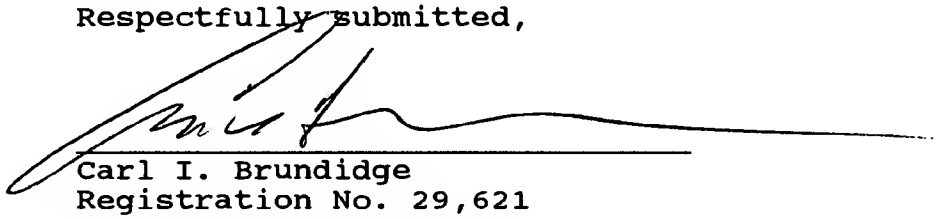
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references

utilized in the rejection of claims 1-12, 14, 16, 18-34 and 44-48.

In view of the foregoing amendments and remarks, Applicants submit that claims 1-12, 14, 16, 18-34 and 44-48 are in condition for allowance. Accordingly, early allowance of claims 1-12, 14, 16, 18-34 and 44-48 is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 C.F.R. section 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (Case No. 500.26967R00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,



Carl I. Brundidge
Registration No. 29,621
ANTONELLI, TERRY, STOUT & KRAUS

CIB/hpg
(703) 312-6600